

What is Claimed is:

1. A method of circuit verification, comprising:

including, in an inductive set of one or more states, a plurality of states of a circuit design, wherein the inductive set of one or more states includes at least states passing a first property of the circuit design;

5 transitioning by at least one step, in a forward direction, states of the inductive set passing at least the first property of the circuit design, resulting in transitioned states;

determining if the transitioned states of the inductive set pass at least the first property of the circuit design; and

repeating at least the transitioning and the determining, until at least, the 10 determining results in the transitioned states of the inductive set passing at least the first property of the circuit design.

2. A method of claim 1, wherein, if all the transitioned states of the inductive set are determined to pass at least the first property of the circuit design, all the transitioned 15 states of the inductive set determined to pass at least the first property of the circuit design were transitioned by a first total of transitions.

3. A method of claim 2, further comprising:

transitioning, in a forward direction, initial states of the circuit design by at least 20 the first total of transitions, resulting in a forward transitioned set of states;

4. A method of claim 3, further comprising:

if the forward transitioned set of states passes the first property of the circuit 25 design, determining the circuit design to be formally verified for at least the first property of the circuit design.

5. A method of claim 1, wherein the determining does not consider transitioned states resulting from transitioning of states of the inductive set failing at least the first property of the circuit design.

6. A method of claim 5, wherein the determining considers only transitioned states resulting from transitioning of states of the inductive set passing at least the first property of the circuit design.

5 7. A method of claim 1, wherein the transitioning is not performed on states of the inductive set failing at least the first property of the circuit design.

8. A method of claim 7, wherein the transitioning is performed only on states of the inductive set passing at least the first property of the circuit design.

10 9. A method of claim 1, wherein, each time the transitioning and the determining are repeated, prior to transitioning, the inductive set includes transitioned states.

15 10. A method of claim 1, wherein, each time the transitioning and the determining are repeated, prior to transitioning, the inductive set includes transitioned states passing at least the first property of the circuit design.

20 11. A method of claim 1, wherein, each time the transitioning and the determining are repeated, prior to transitioning, the inductive set excludes transitioned states failing at least the first property of the circuit design.

12. A method of circuit verification, comprising:  
transitioning by at least one step, in a backward direction, states of an inductive set of at least one or more states of a circuit design passing at least a first property of the circuit design, resulting in transitioned states;  
determining if the transitioned states of the inductive set fail at least the first property of the circuit design; and  
repeating the transitioning and the determining, until at least, the determining results in the transitioned states of the inductive set failing at least the first property of the circuit design.

13. A method of claim 12, further comprising:

5 a first iteration of transitioning by at least one step, in the backward direction, states of a first iteration of an inductive set of at least one or more states failing at least the first property of the circuit design, resulting in a first iteration of transitioned states.

14. A method of claim 13, further comprising:

10 a first iteration of determining if the first iteration of transitioned states of the inductive set fail at least the first property of the circuit design;

15. A method of claim 14, wherein, after the first iteration of transitioning, prior to the transitioning, the inductive set includes the first iteration of transitioned states.

16. A method of claim 14, wherein, after the first iteration of transitioning, prior to the transitioning, the inductive set includes the first iteration of transitioned states passing at 15 least the first property of the circuit design.

17. A method of claim 14, wherein, after the first iteration of transitioning, prior to the transitioning, the inductive set excludes the first iteration of transitioned states failing at 20 least the first property of the circuit design.

18. A method of claim 12, wherein, at least after a first iteration of transitioning, the determining does not consider transitioned states resulting from transitioning of states of the inductive set failing at least the first property of the circuit design.

25 19. A method of claim 18, wherein, at least after a first iteration of transitioning, the determining considers only transitioned states resulting from transitioning of states of the inductive set passing at least the first property of the circuit design.

30 20. A method of claim 19, wherein, at least after a first iteration of transitioning, the transitioning is not performed on states of the inductive set failing at least the first property of the circuit design.

21. A method of claim 20, wherein, at least after a first iteration of transitioning, the transitioning is performed only on states of the inductive set passing at least the first property of the circuit design.

5 22. A method of claim 12, wherein, at least after a first iteration of transitioning, each time the transitioning is repeated, prior to the transitioning, the inductive set includes transitioned states.

10 23. A method of claim 12, wherein, at least after a first iteration of transitioning, each time the transitioning is repeated, prior to the transitioning, the inductive set includes transitioned states passing at least the first property of the circuit design.

15 24. A method of claim 12, wherein, at least after a first iteration of transitioning, each time the transitioning is repeated, prior to the transitioning, the inductive set excludes transitioned states failing at least the first property of the circuit design.

20 25. A method of claim 12, wherein, at least after a first iteration of transitioning, each time the transitioning is repeated, prior to the transitioning, the inductive set excludes transitioned states able to reach, in one forward transition, any state of the circuit design failing at least the first property.

25 26. A method of claim 12, wherein, at least after a first iteration of transitioning, each time the transitioning is repeated, prior to the transitioning, the inductive set includes transitioned states except for transitioned states able to reach, in one forward transition, any state of the circuit design failing at least the first property.

30 27. A method of claim 12, wherein, at least after a first iteration of transitioning, each time the transitioning is repeated, prior to the transitioning, the inductive set includes transitioned states passing at least the first property of the circuit design except for transitioned states able to reach, in one forward transition, any state of the circuit design failing at least the first property.

28. A method of claim 12, wherein, at least after a first iteration of transitioning, each time the transitioning is repeated, prior to the transitioning, the inductive set excludes transitioned states failing at least the first property of the circuit design and transitioned states able to reach, in one forward transition, any state of the circuit design failing at least the first property.

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29. A method of circuit verification, comprising:

attempting bounded verification of one or more properties of a circuit design for at least a first number of transitions;

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attempting induction proof of the one or more properties of the circuit design for at least the first number of transitions; and

determining if the one or more properties of the circuit design are verified, based at least on the bounded verification and the induction proof.

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30. The method of claim 29, further comprising:

if the bounded verification and the induction proof are insufficient to determine the one or more properties of the circuit design to be verified, increasing the first number of transitions;

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repeating at least one of attempting bounded verification and attempting induction proof; and

determining if the one or more properties of the circuit design are verified, based at least on repeating, with the increased first number of transitions, at least one of bounded verification and the induction proof.

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31. A method of circuit verification, comprising:

a first iteration of transitioning by at least one step, in a backward direction, states of a first iteration of an inductive set of at least one or more states failing at least a first property of a circuit design, resulting in a first iteration of transitioned states.

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a first iteration of determining if the first iteration of transitioned states of the inductive set fail at least the first property of the circuit design.